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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,599	11/20/2003	Herman Kwong	57983.000119	7194

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EXAMINER	
ARBES, CARL J	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/716,599	KWONG ET AL.	
	Examiner	Art Unit	
	C. J. Arbes	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date herein
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Applicants' Remarks filed on or about 05 January 2006 have been duly considered but are held not to justify or overcome the Office's position or holding with respect to the Office's Restriction. That is Applicants *inter alia* opine that for a valid Restriction the inventions must be separate and distinct. Applicants are or should be aware of what or how the Office for many or untold number of years construes this language to include i.e. separate or distinct. Even assuming arguendo that Applicants are correct on this count nevertheless the Restriction, which was mailed on or about 13 December 2005 has not been satisfactorily rebutted by Applicants. The reason for the original Restriction should have been reviewed. That is in the Group II invention there is no requirement that a "forming step ..." be used to form a signal routing channel as there is in the Group I invention and this reason should been provided in the original Restriction. The forming step in the Group II invention could have taken place when the substrate was being fabricated. The Restriction is proper and is now **made Final** although the technical reason therefore was not clear as it is now. Applicants are required to cancel all non-elected claims or take other appropriate action.

An Office Action on the merits of Claims 1-10 follows

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ball et al. (Pat No 6,246,112 B1) hereinafter Ball et al

Ball et al teach a method of routing signal traces in an electronic device package which includes the acts of disposing a plurality of signal traces on at least one substrate layer, and interleaving a plurality of ground traces with the signal traces. Ball et al also teach providing plurality of components on the surface of a multi-layered signal routing device (Cf. Figures 3-5 and corresponding disclosure). One can infer or understand (from at least viewing Figure 5), if indeed Ball et do not expressly teach that at least a signal routing channel on at least a surface of the multi-layered device is greater than a component space that from at least Figures 3 and 4 it is seen that Ball et al indeed teach providing micro-vias for the multi-layered signal routing device and also a plurality of conducting pads particularly seen in Figure 4 and moreover it would have been obvious if indeed Ball et al do not specifically teach to provide a signal routing channel which has a channel space which is equal to or greater than the component space. (Cf e.g. Figure 5 in combination with Figures 3 and 4). As specifically to claim 2 iot is held that an act of ... determining a number... or ...determining aa required space.. is merely mental and hence will be little or no patentable weight since these steps are not within the requirements of further narrowing the scope of the independent claim 1. As applied To claim 3 it is held that one does have or can have a routing channel on a secondary surface of the multi-layer device given the evidence in Ball et al if one construes the bottom layer of Figures 3 or 4 as the secondary surface. One can readily see from each of these Figures that the vias or microvias do indeed extend from the top of the multilayer device to the bottom of the device and obviously components can be attached to this secondary surface. As applied to Claims 5 and 7 although Figures 3

and 4 do not show conductive pads on the bottom of these Figures it would be just a matter of mere design choice to place conductive pads on the bottom since there is no specific proble which is being solved by such pad being placed on the secondary surface nor is there any particular purpose therefore. Furthermore it would have been obvious to a POSITA to indeed place pads on this secondary surface. As applied to Claims 6 and 9 similar considerations apply. That is the placement of a portion of the plurality of components on the secondary surface rather than what Ball et al i.e. placement of each of the components on a primary surface is mere design choice for the reasons already provided. Alternatively the fictitious POSITA without undue skill would place components on the surface given the evidence in Ball et al.

Claims 1 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Haller et al (Patent No. 5,357,403); hereinafter Haller et al.

Haller et al teach micropositioning of chips in an high density interconnect structure which has an alignment conductor in the high density interconnect structure. The alignment levels of such a structure are preferably a ground plane and if two layers of alignment conductors are provided, a power plane. Haller al therefore teaches a multi-layer device for accommodating a plurality of components on a surface. (Cf. Background of the Invention in Col 1) . From at least Figure 1 and corresponding disclosure it is seen or inferred that a signal routing channel is or can be provided on the surface and that the signal routing channel has a channel space that is greater than the component space. It is also evident from at least from Figures 2, 4, 6 and 8 that Haller et al provides microvias in the multi-layered routing device (N.B. The only reason that

the Office will not reject Claims 1-5 and 10 under 35 U.S.C 102 b) is that Haller et al do not expressly state that they form at least one signal routing channel on at least the surface of the multi-layer signal routing device, the at least one signal routing channel ... . However this is exactly what Haller et al do with the high density interconnection which they disclose. As applied to Claim 7 at least in Figs. 2, 6, 8, 10 and 12 the elements 18, near 34 and near A clearly show conductive pads which are formed on the secondary surface of the multi-layer signal; routing device. As applied to claim 9 as was the case with respect to this claim as rejected hereinabove the same or similar rationale is applied to wit the claim limitation is held to be mere design choice or alternatively would have been obvious to a POSITA.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to C. J. Arbes whose telephone number is 571-272-4563. The examiner can normally be reached on M, T, R and F from 8 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, P. Vo, can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. J. Arbes
Primary Examiner
Art Unit 3729